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METHOD AND SYSTEM FOR PROVIDING A VIDEO SIGNAL

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PATENT APPLICATION

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METHOD AND SYSTEM FOR PROVIDING A VIDEO SIGNAL

Field of the Invention

The present invention relates generally to providing video signals, and more specifically to providing multiple video signals using a single tuner.

Background of the Invention

The use of multiple tuners in video applications to provide such functions as picture in a picture (PIP) is well known. By providing such capabilities, it is possible for a user to monitor multiple channels simultaneously.

In order to display simultaneous full motion video images, playback devices, such as televisions, have to incorporate multiple tuners. The multiple tuners may be incorporated within an individual playback device, or may be in external devices, such as video cassette recorder, whereby the external device provides the a received signal the playback device.

The use of multiple tuners within a television increases the overall cost of a system. Cabling and associated connectors increase the cost of systems where an external tuner is used to provide a received signal to a television to provide the second full motion video image. The use of an external tuner further requires the use of multiple control

devices, such as remote controls, to control each of the tuning devices. Multiple tuners within a television inherently increase the cost of the system. The increased complexity of such systems is disadvantageous. Therefore, a method and system for overcoming the disadvantages of the prior art systems would be advantageous.

Brief Description of the Drawings

Figure 1 illustrates, in block diagram form, a system in accordance with the present invention;

Figure 2 illustrates, in block diagram form, the tuner of Figure 1 in greater detail;

Figure 3 illustrates, in time line form, when fields of video data are transmitted;

Figure 4 illustrates, in graphical form, a composite video signal;

Figure 5 illustrates, in block diagram form, an alternative implementation of the tuner of Figure 1;

Figure 6 illustrates, in block diagram form, an alternative implementation of the tuner of Figure 1; and

Figures 7 and 8 illustrate, in flow diagram form, specific implementations of the method of the present invention.

Detailed Description of the Drawings

In accordance with a specific embodiment of the present invention, a tuner alternates between receiving a first video signal and a second video signal, such that every other frame or field of video data is received for each specific signal. The signals are alternatively received by providing alternating data values in each of an IF1 and IF2 control register. The values are switched during the vertical blanking interval of the received data. Subsequently, the video images are displayed in full motion video by

interpolating the missing fields of data not received by the tuner.

The present invention is best understood with reference to the figures. Figure 1 illustrates a block diagram of a system in accordance with the present invention. Figure 1 includes an antennae 105 connected to a tuner 110. The tuner 110 is connected to an analog-to-digital converter 112. The analog-to-digital converter 112 is connected to the video decoder 114. The video decoder 114 is connected to the memory 116. Memory 116 is connected to display engine 118. The display engine 118 is connected to the display device 120.

In operation, the tuner 110 receives a signal from antennae 105. Generally, the signal received from antennae 105 would be understood to include composite signals of the type associated traditionally transmitted video signals. However, it would be understood that the antennae 105 can also represent signals received in a compressed or uncompressed form, from other media, including the internet, and other transmission media whereby multiple signals are transmitted at various frequencies.

The tuner 110 selects one of the plurality of received signals based upon information received across the bus 130. By receiving a plurality of information across the bus 130, it is possible for the tuner 110 to switch between a plurality of frequencies, thereby allowing the tuner 110 to provide the information necessary to display a plurality of video images on the display device 120. The information provided by the tuner 110 is provided to the analog to digital converter 112. The analog-to-digital converter 112 converts the received analog signals into a digital format. The converted digital information is provided to the video decoder 114.

The video decoder 114 decodes the digital information from it retrieved format into a digital data of a chosen protocol. Such protocols include such as a YUV color space protocol, or an RGB color space protocol. The decoded information generated by the video decoder 114 is stored via bus 140 in memory 116. Note that additional processing of the decoded signal can occur between the actual decoding of the data and its storage in the memory 116.

Once stored in memory 116, the display engine 118 accesses the memory 116 to retrieve the stored image and provide it to the display device 120. As discussed previously, with reference to the tuner 110, data representing multiple images is being received by the tuner 110, which represent a single tuner. The received information is stored in separate locations within the memory 116.

In a specific implementation, where the tuner 110 is alternatively receiving fields of data on multiple channels, it is be necessary for the video decoder, or some other portion of the system, to interpolate the missing image data. For example, where the tuner 110 alternates receiving fields from a first frequency (associated with a first channel) and a second frequency (associated with a second channel), only every other field of a given channel will be provided by the tuner 110. Therefore, it is necessary for the video decoder, or some other portion of the graphics adapter, to interpolate the missing image data based upon the received data alternating received fields. Examples of such techniques, which are well know, and include vertical filtration.

Fields associated with a plurality of full motion video channels are stored in memory 116 for retrieval by the display engine 118. When displayed upon the display device 120, multiple channels of video can be viewed. Generally, the multiple channels are displayed in separate windows where a computer monitor is being used.

Figure 2 illustrates in block diagram form a portion of the tuner 110 in accordance with the present invention. Specifically, the portion of the tuner illustrated in Figure 2 includes mixers 212 and 216, a band-pass filter 214 for performing band-pass filtering, a control portion 217, and a tuning portion 230.

In operation, the signal received from antennae 105 is combined at mixer 212 with a frequency provided by the tuning block 230. The output signal of the mixer 212 is provided to the filter block 214. The band-pass filter 214 will provide a selected channel frequency. By appropriately filtering the received signal, a specific portion of the received signal can be further processed. The filtered signal from band-pass filter 214 is provided to mixer 216, which receives a frequency from the tuning block 230. The

output of the mixer 216 provides a desired IF frequency. Note the frequencies provided by the tuning block 230 determine the actual channel frequency selected. The output if mixer 216 is received by control portion 217, which provides various control functions to the tuning portion 230.

The tuning portion 230 comprises a frequency generation block 218 containing multiple frequency generators. Each of the frequency generators of portion 218 receive a frequency value. The frequency values are stored in registers 220 and 222 for specifying the IF1 and IF2 frequency values respectively.

Figure 3 is a time line indicating the sequence during which individual fields are received by the antenna 105. Video images include a plurality of sequential fields. By displaying the plurality of sequential frames at an appropriate rate a full motion video image is produced. Note that the channel value X is a function of the IF1 and IF2 frequency values. By providing specific IF1 and IF2 frequencies, a specific channel X can be selected.

Each frame is transmitted as two fields. Separate fields are utilized in order to improve video quality by accommodating the interlacing of images. Therefore, referring to Figure 3, F1A and F1B represent two fields (A and B) associated with the frame 1 (F1) of channel X. Likewise, F2A, and F2B represent the two fields associated with a frame 2 of channel X.

Figure 4 illustrates a the vertical blanking interval associated with an NTSC composite video format. Time periods 1-3 represent the final three fields associated with a particular frame. Time periods 4-24 represent the vertical blanking interval (VBI), which includes various equalization and serration pulses (not specifically illustrated). The vertical blanking interval, in Figure 4 is of specific interest because in a specific implementation of the present invention the tuner is changed during the VBI interval.

Referring back to Figure 2 and assuming two channels are to be provided by the tuner 110, the IF1 control register and IF2 control register are loaded with the appropriate

IF1 and IF2 values to tune into a first selected channel. In a specific embodiment, the values contained within IF1 control register and IF2 control register will be changed at a frequency allowing for adjacent fields of different channels to be received. In other words, referring to Figure 3, the active video of a first channel will be received during time T1, and the active video for a second channel will be received during time T2

In order to accomplish receiving adjacent fields, one set of control register values would be stored in order to receive a first channel, and just prior to the second time, a second set of IF1 and IF2 control register values will be stored within the registers 220 and 222 in order to receive the field F1B associated with a second channel. In an alternating manner, the value stored within the control registers IF1 and IF2 are be changed in order to receive alternating field from each of the first and second frequency.

In an alternate embodiment, it would be understood that instead of receiving alternating fields, it would be possible to receive alternating frames. In this manner, when tuned to a first frequency, the fields F1A and F1B would be received by the tuner 110. Subsequently, the values associated with the control registers of IF1 and IF2 would be updated to reflect the second channel whereby the field F2A and field F2B of the second frame for the second channel would be received.

In addition, it is understood by one skilled in the art that in addition to receiving adjacent fields associated with a single frame, such as from T1 to T3, it would be possible to receive adjacent fields associated with different frames. In other words, frame F1B and F2A could be received for a single channel in an alternating manner. As previously discussed, interpolation techniques can be used in order to fill in the missing data in order to accommodate the display of full motion video.

In order to accommodate the rapid tuning from one channel to another, a fast tuner, such as a solid state tuner, should be used. However, the solid state tuners available support a slow bus interface protocols over the bus 130, see Figure 1, to set the values of IF1 register and the IF2 register. Therefore, either a faster bus interface over the

bus 130 needs to be used, or alternate techniques within the tuner 110 need to be used in order to support the rapid switching between channels.

In one implementation, the bus interface 130 of Figure 1 is a bus interface capable of supporting high speed transfers of data directly to the IF1 and IF2 control registers 220 and 222. Currently, the bus 130 is an I²C bus interfaces, which is too slow to accomplish the present invention by directly writing to the register. Therefore, other proprietary or standard bus interfaces protocols capable of changing data fast enough to allow tuning into multiple channel would need to be used. Such a bus would have approximately 1.2 milliseconds to write the data and acquire locking. While possible with very fast three wire busses, or other multiple data bit protocols, such high rates may be impractical.

Figure 5 illustrates another implementation of the tuning block 230 of Figure 2 in accordance with the present invention. Figure 5 allows for an IF1 prelude register, and an IF2 preload register to allow for rapid change of the IF values of the actual control registers 220 and 222. In this implementation, the traditional I²C bus protocol, or virtually any other bus protocol, can be used to load data into the IF1 and IF2 prelude register at any time. Once the vertical blanking interrupt a signal is detected, or other desired event, a load signal is generated in order to rapidly load the value stored preload values into the IF1 and IF2 control registers 220 and 222 respectively. Once loaded, the frequency generator 118 will generate and provide new frequencies to the mixers 112 and 116 of Figure 2. Noted that detection of the vertical blanking interrupts signal can be accomplished through the control portion 117 of Figure 2 which in turn would provide the load signal to the IF1 and IF2 control registers of Figure 5. One advantage of the implementation of Figure 5, is that it allows for the traditional I²C interface to be used since the new channel can be loaded over a longer period of time.

Figure 6 illustrates another implementation in accordance with the present invention. In Figure 6, there is a set of channel 1 control registers 610 and a set of channel 2 control registers 620. Each of the register sets 610 and 620 include an IF1 register as well as an IF2 register. The IF1 registers of both channel 1 and channel 2 are

provided to a multiplexor 630. Likewise, the IF2 registers of channel 1 and channel 2 are provided to a multiplexor 631. A common channel select signal is received by each of the multiplexors 630 and 631. When in a first state, the channel 1 controller register values are provided to the frequency generator 618. When the channel select is in a second state, the channel 2 control register values are provided to the frequency generator 618. In this manner, it is possible to load the channel 1 and channel 2 control registers 610 and 620 with data, and other control information, in order to provide for rapid switching between selected channels. As previously discussed, the control portion 117 can used in order to monitor the received signals to determine when a vertical blanking interrupt, or other appropriate signal event, occurs to switch between the selected channels.

Figure 7 illustrates a method in accordance with the present invention. At step 701, the receiver is tuned to a first frequency. As discussed previously, this is accomplished by providing an IF1 control register value, and an IF2 control register value. Based upon the IF1 and IF2 control registers values, a specific channel of video can be received by the tuner.

At step 702, a first field of video associated with the first frequency is received. As discussed with reference to Figure 3, a field of video is described to be at least a portion of a frame of video. Whereby a frame of video represents an entire screen of information.

At step 703, the receiver is tuned to a second frequency. In a specific implementation, this occurs during the vertical blanking interval of the composite signal. When provided during the vertical blanking interval, the step of providing needs to occur in less than approximately 1.2 milliseconds. During this time period Phase Locked Loop settling should occur.

At step 704, a second field of video associated with the second frequency is received. The first frame of video and the second frame of video are adjacent in time. Referring to Figure 3, adjacent in time for fields of different frequencies means receiving

a first field of video during time T1 for a first frequency, and a field at time T2 for a second frequency.

At step 705 the first field of video is displayed. It should be noted, that the first field of video may actually include interpolated data from previously or subsequently received frames or fields of data.

At step 706, the receiver is tuned to the first frequency after the step of receiving the second field.

At step 707, a third field associated with the third frequency is received.

At step 708, the third field is displayed, wherein the first field and the third field are associated with adjacent frames of a common video image. Referring to Figure 3, adjacent video image fields would include F1A and F2A. In other words, the first frame would include fields transmitted from time T1 through time T2, while the second adjacent frame associated with full motion video would include fields transmitted from time T3 through time T4.

At step 709, the second field, is displayed in an area of the display device that is substantially mutually exclusive from the first image. In other words, the second image is displayed in a separate window, or a separate portion of the screen from the first image, such that the first image and the second image can be displayed simultaneously on a single display device, or on multiple display devices simultaneously.

The present invention provides an advantage over the prior art in that it allows for multiple video signals to be received using a single tuner. The multiple images can be displayed simultaneously on a single device, such as in a picture in a picture format, or on separate display devices. Being able to control a tuner that can receive multiple images simultaneously is an advantage over the prior art, in that it reduces the need for a second tuner whether associated with the television, or with an associated video cassette recorder as discussed previously. One of ordinary skill in the art will understand that various

implementations of the present invention can implemented without departing from the scope of the claimed invention herein.